REMARKS

I. Introduction

In response to the Office Action dated January 17, 2006, Applicants have amended claims 1 and 11 to more particularly point out and distinctly claim the subject matter of the present invention. No new matter has been added. In view of the foregoing amendments and the following remarks, Applicants respectfully submit that all pending claims are in condition for allowance.

II. Claim Rejections Under 35 U.S.C. § 102

Claims 1 – 6 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent Publication No. 2003/0041224 to Toda. Applicants traverse this rejection for at least the following reasons.

Claim 1, as amended, recites a timing signal output circuit for outputting a timing signal indicative of a timing that is shifted by a predetermined time period, which is determined according to a frequency of the clock signal and a read data control circuit for performing control such that the microcomputer takes in the data read from the memory based on the timing signal only when the clock signal has a predetermined frequency between an upper limit and a lower limit determined according to the shift of the timing. At least these features are not disclosed by Toda.

Toda appears to disclose a memory board system wherein the timing at which a memory module outputs data is adjusted in accordance with the timing at which the data arrives at the controller. This timing adjustment, however, is not determined based on a frequency of the clock signal, as recited in claim 1. Furthermore, Toda is silent regarding controlling the

microcomputer such that the microcomputer takes in data read from the memory based on the timing signal only when the clock signal has a predetermined frequency between an upper and lower limit, which is determined according to the shift of the timing.

As anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, *713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983)*, and Toda fails to disclose at least the foregoing claim elements, it is clear that Toda does not anticipate amended 1.

III. Claim Rejections Under 35 U.S.C. § 103

Claims 7 – 8 and 11 – 12 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Toda in view of U.S. Patent Application Publication No. 2003/0233562 to Chheda. Claim 9 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Toda in view of U.S. Patent No. 6,002,627 to Chevallier. Claims 10 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Toda in view of U.S. Patent No. 6,437,308 to Koh. Applicants traverse these rejections for at least the following reasons.

Claim 11, as amended, recites among other things, a timing control circuit for performing control such that the predetermined time period during which the mask circuit outputs the data read from the memory and the timing for taking the data output from the mask circuit into the microcomputer correspond to each other and are variable. The Examiner acknowledges that Toda fails to disclose a mask circuit as recited in claims 7 and 11, and relies on Chheda to overcome this deficiency. However, neither Toda nor Chheda, alone or in combination with each other, teach or suggest performing control between the predetermined time period which the

mask circuit outputs data from the memory and the timing for taking the data output into the microcomputer such that they correspond to each other and are variable, as recited in claim 11.

Chheda appears to disclose a data protection circuit for allowing access to data stored in memory. The circuit may include a mask circuit which appears to enable a read or write signal to the memory to be disabled. However, Chheda does not disclose a timing control circuit which controls the predetermined time period during which the mask circuit outputs the data read from the memory and the timing for taking the data output from the mask circuit into the microcomputer such that they correspond to each other and are variable.

Even if the mask circuit of Chheda could be combined with the teachings of Toda, there is no teaching or suggestion in either reference, taken alone or in combination with each other, of a timing control circuit as recited in claim 11 which controls the predetermined time period during which the mask circuit outputs the data read from the memory and the timing for taking the data output from the mask circuit into the microcomputer such that they correspond to each other and are variable.

Accordingly, as each and every limitation must be disclosed or suggested by the prior art references in order to establish a *prima facie* case of obviousness (MPEP § 2143.03), and the combination of Toda and Chheda fails to do so, it is respectfully submitting that claim 11 is patentable over Toda and Chheda taken alone or in combination with one another.

IV. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,*

819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims and 11 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

V. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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